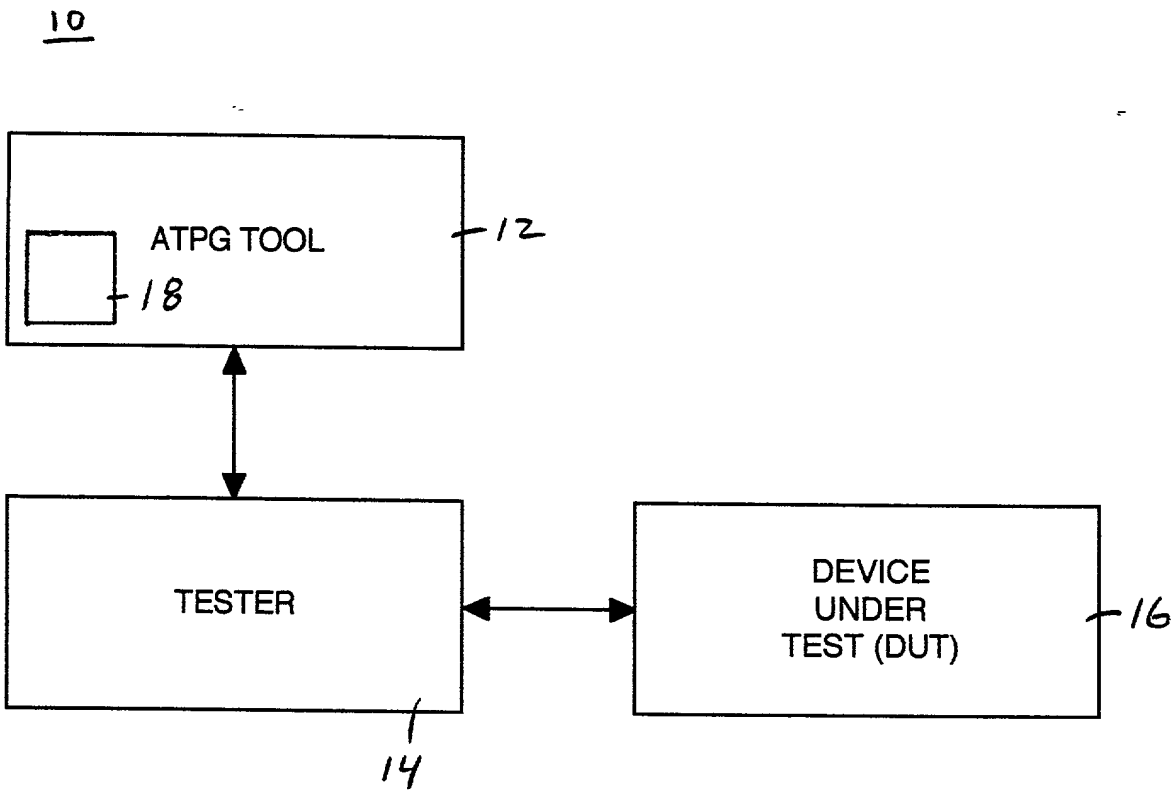

FIG. 1

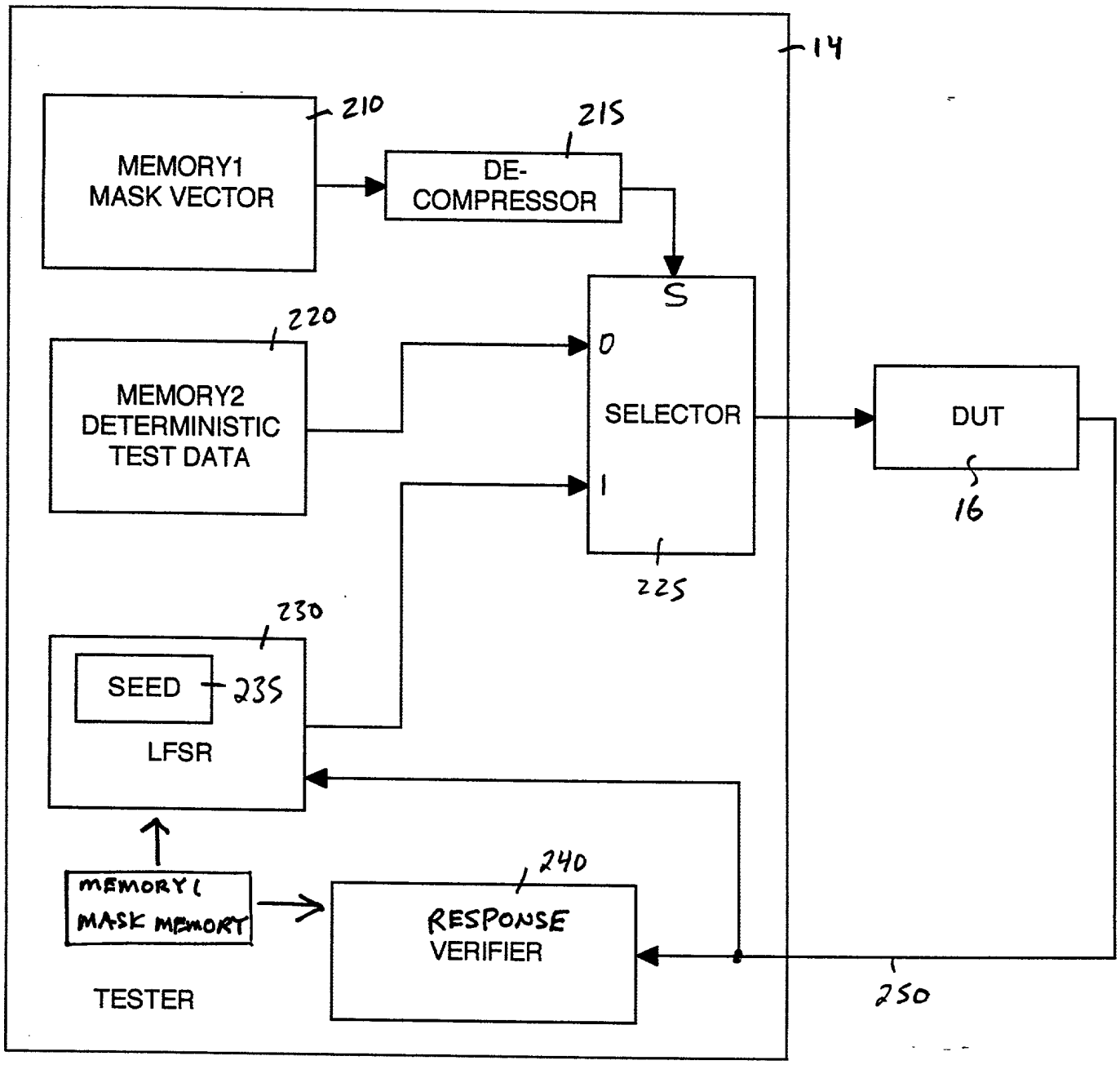
14
210
MEMORY1
MASK VECTOR
215
DE-
COMPRESSOR
S
220
MEMORY2
DETERMINISTIC
TEST DATA
0
SELECTOR
1
225
DUT
16
230
SEED
235
LFSR
MEMORY1
MASK MEMORY
240
RESPONSE
VERIFIER
TESTER
250

FIG. 2

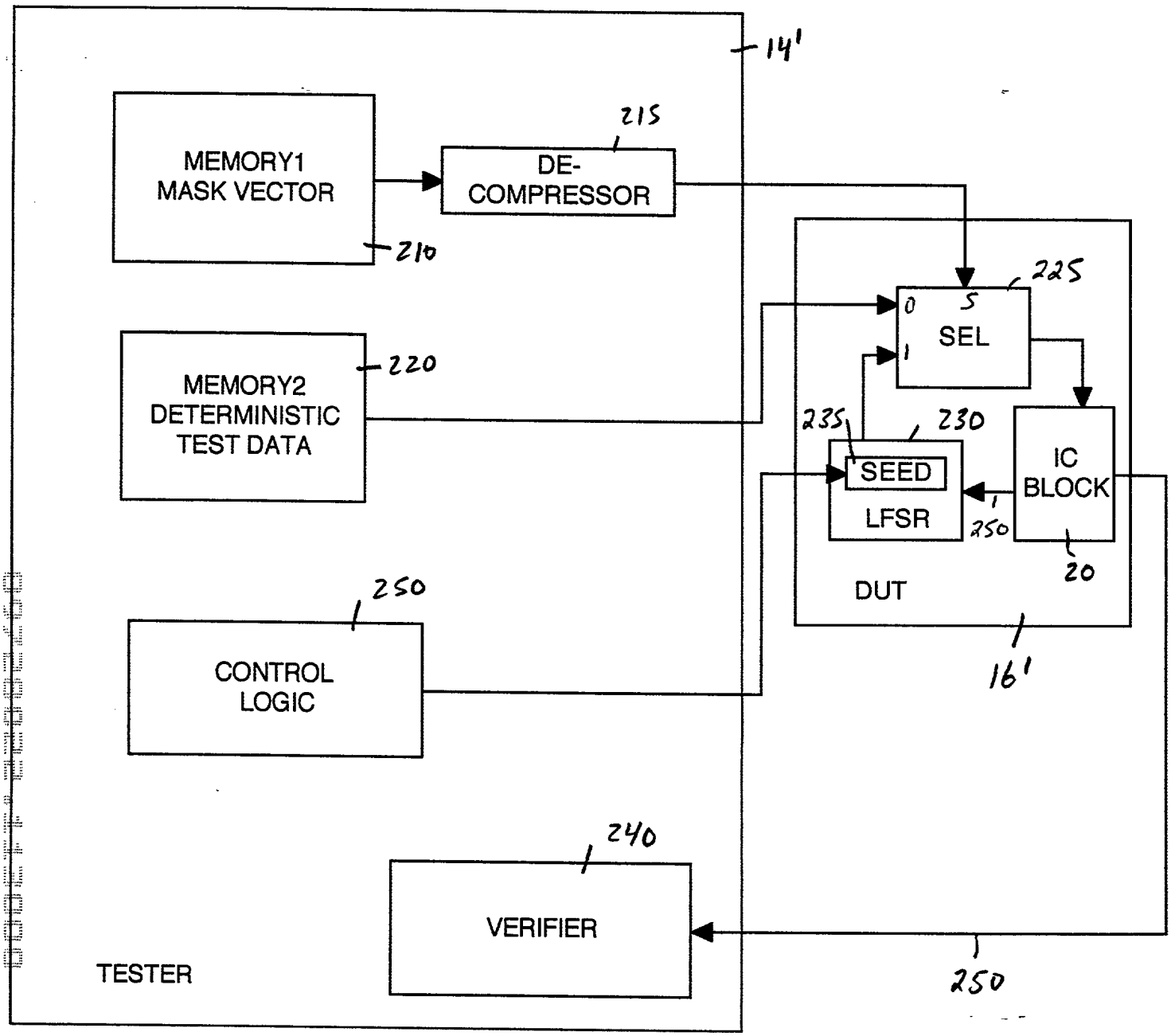
14'
MEMORY1
MASK VECTOR
210
215
DE-
COMPRESSOR
225
0
5
SEL
1
MEMORY2
DETERMINISTIC
TEST DATA
220
235
230
SEED
LFSR
IC
BLOCK
250
20
DUT
16'
250
CONTROL
LOGIC
240
VERIFIER
TESTER
250

FIG. 3

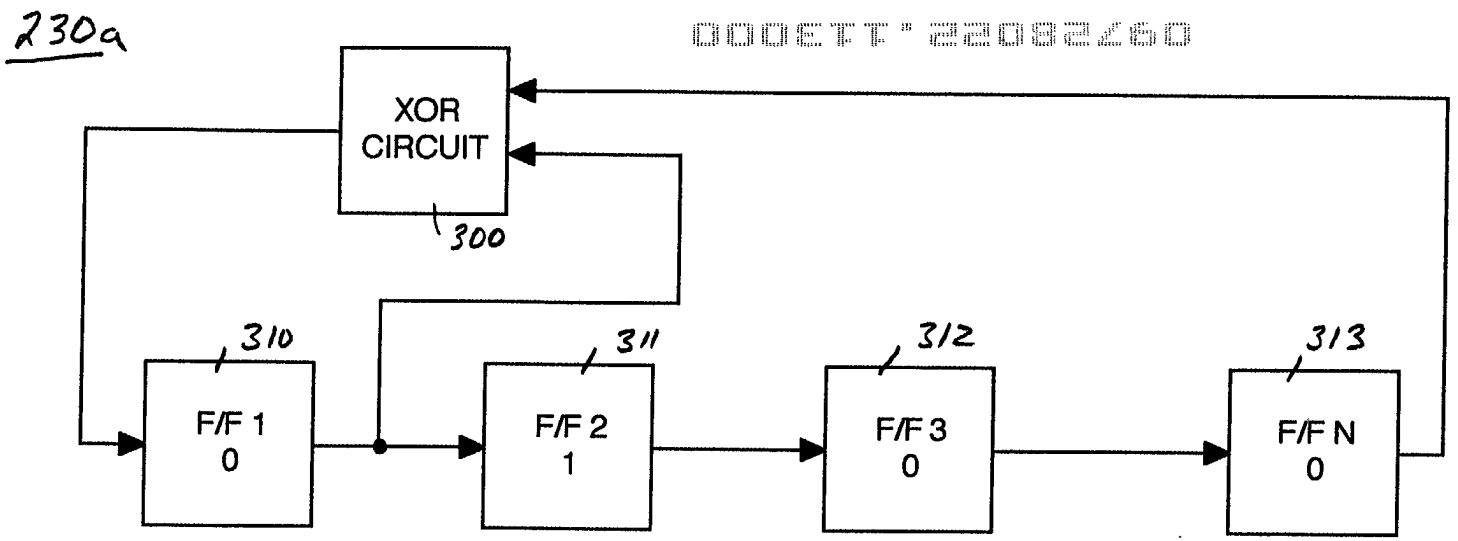

FIG. 4A

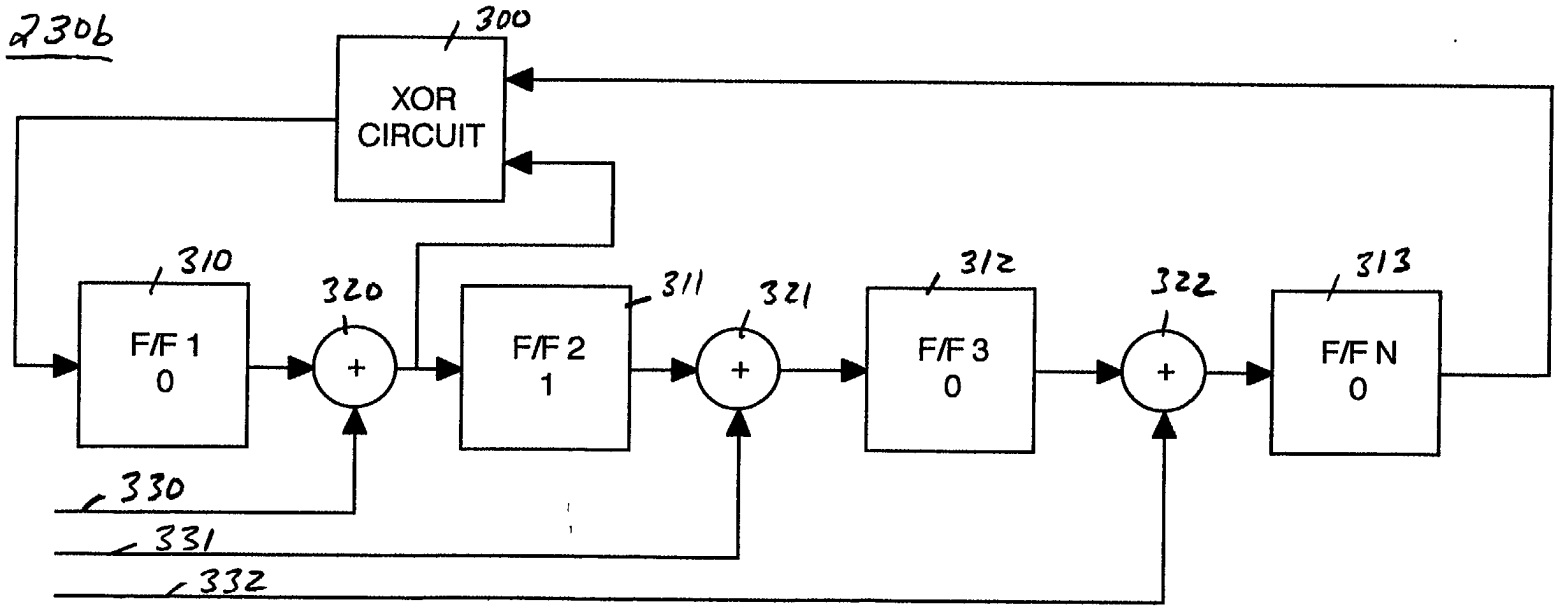

FIG. 4B

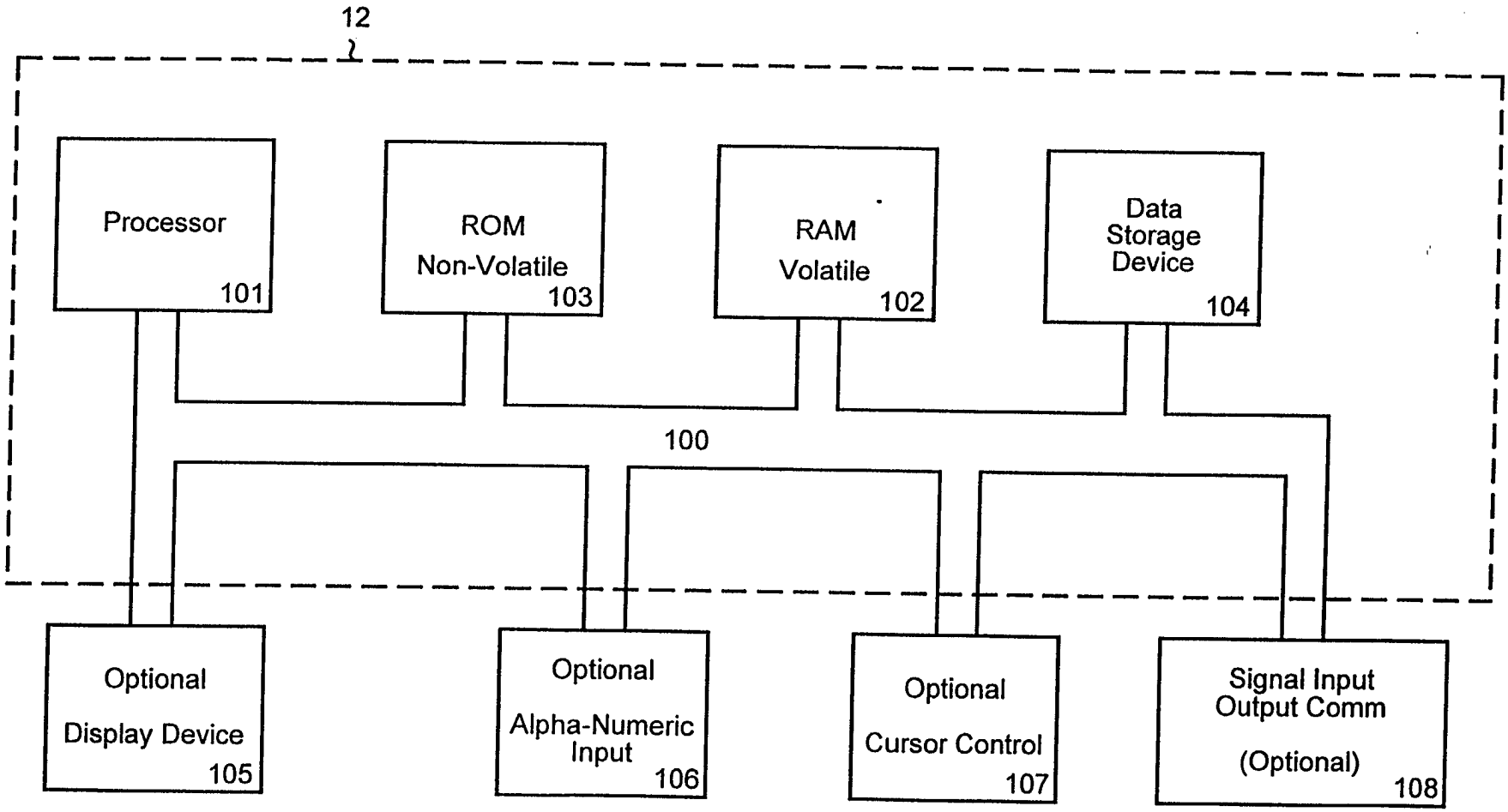

FIG. 5

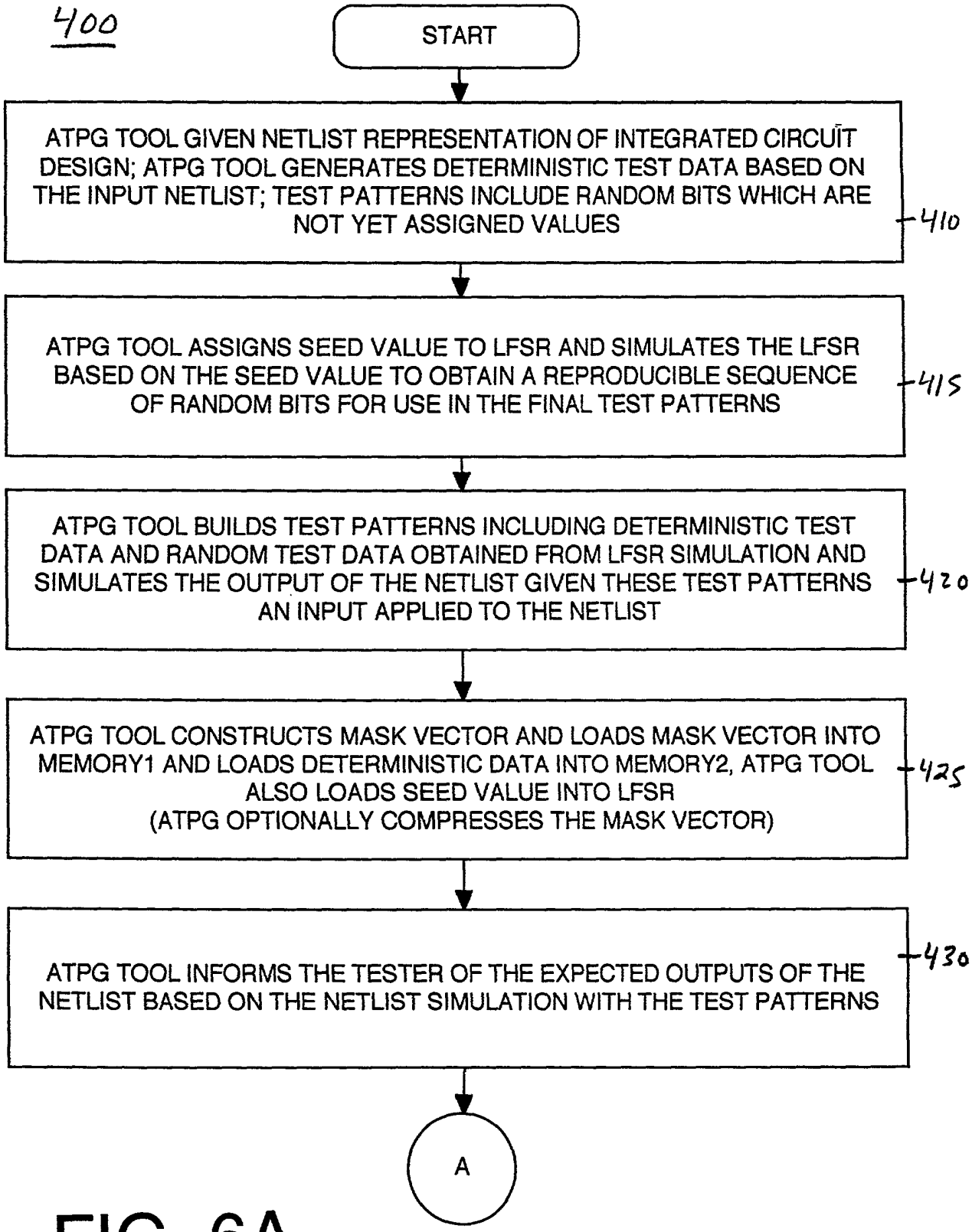
400
START
ATPG TOOL GIVEN NETLIST REPRESENTATION OF INTEGRATED CIRCUIT DESIGN; ATPG TOOL GENERATES DETERMINISTIC TEST DATA BASED ON THE INPUT NETLIST; TEST PATTERNS INCLUDE RANDOM BITS WHICH ARE NOT YET ASSIGNED VALUES
410
ATPG TOOL ASSIGNS SEED VALUE TO LFSR AND SIMULATES THE LFSR BASED ON THE SEED VALUE TO OBTAIN A REPRODUCIBLE SEQUENCE OF RANDOM BITS FOR USE IN THE FINAL TEST PATTERNS
415
ATPG TOOL BUILDS TEST PATTERNS INCLUDING DETERMINISTIC TEST DATA AND RANDOM TEST DATA OBTAINED FROM LFSR SIMULATION AND SIMULATES THE OUTPUT OF THE NETLIST GIVEN THESE TEST PATTERNS AN INPUT APPLIED TO THE NETLIST
420
ATPG TOOL CONSTRUCTS MASK VECTOR AND LOADS MASK VECTOR INTO MEMORY1 AND LOADS DETERMINISTIC DATA INTO MEMORY2, ATPG TOOL ALSO LOADS SEED VALUE INTO LFSR
(ATPG OPTIONALLY COMPRESSES THE MASK VECTOR)
425
ATPG TOOL INFORMS THE TESTER OF THE EXPECTED OUTPUTS OF THE NETLIST BASED ON THE NETLIST SIMULATION WITH THE TEST PATTERNS
430
A

FIG. 6A

400 cont

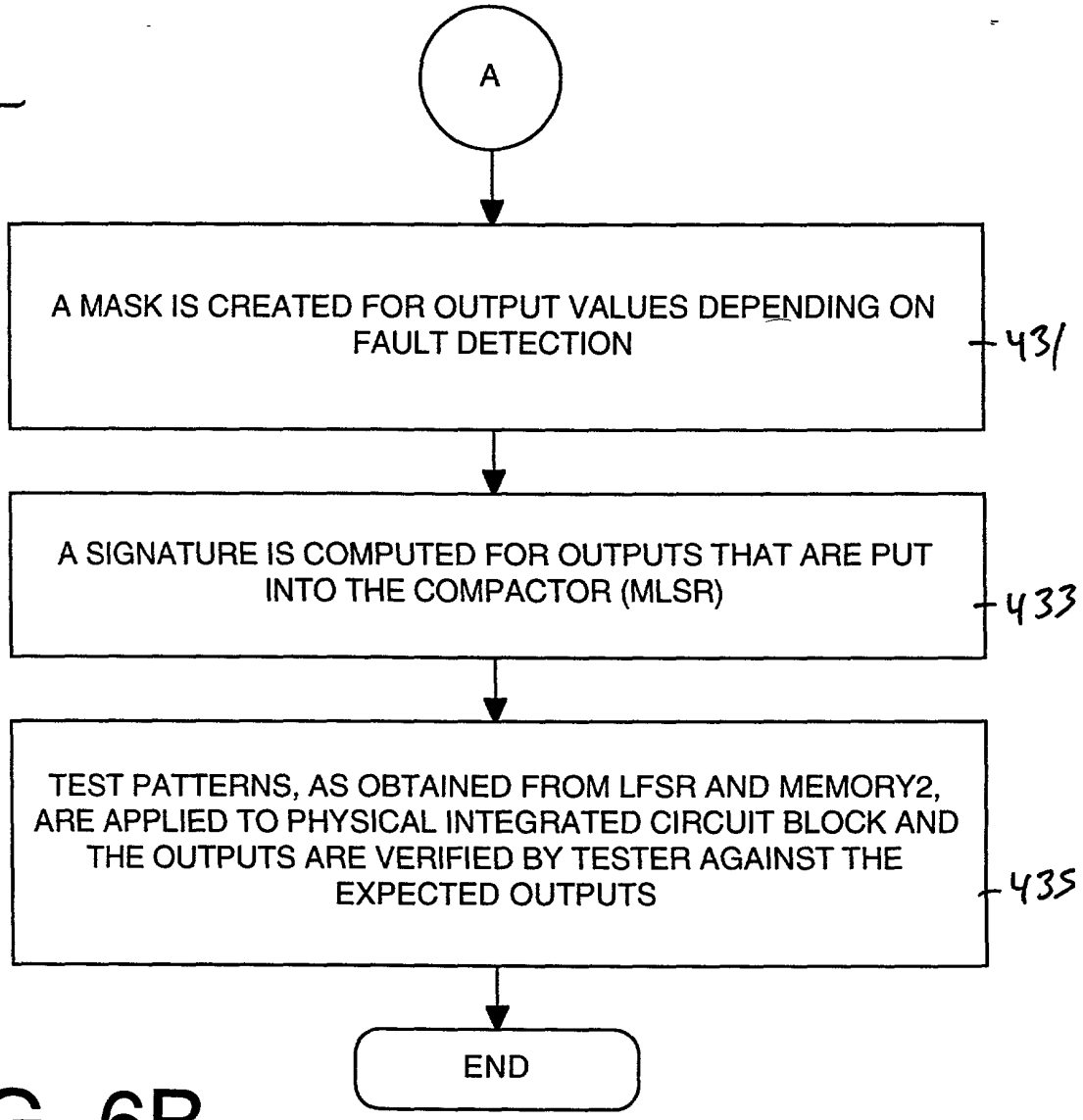

FIG. 6B

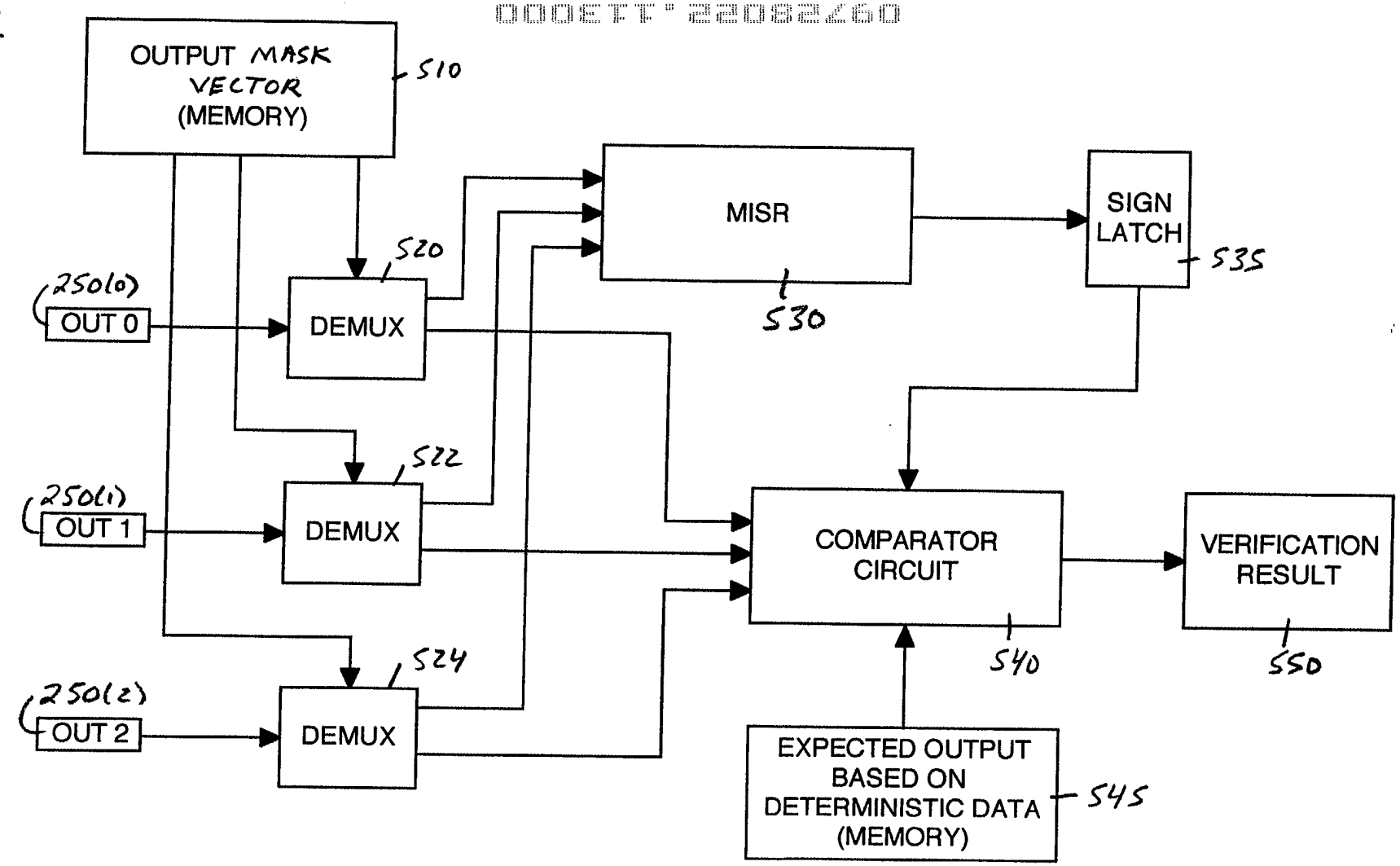

FIG. 7